CLAIMS

Claim1. An ohmic resistor comprising:

MOSFET having a drain, a source and a gate;

a dc voltage applied across said MODFET between said rain and said source;

a dc drain current flowing from the drain to the source; and

an adaptive gate voltage appearing automatically at said gate such that the MOSFET operates in the ohmic region of the drain V-I characteristic.

Claim 2. The ohmic resistor as described in claim 1, wherein nothing is connected to said gate.

Claim 3. The ohmic resistor as described in claim 2, further comprising resistance mirror to mirror the resistance of said ohmic resistance, comprising:

more than one MOSFETs having a common source, a common floating gate and separate drains.

Claim 4. The ohmic resistor as described in claim 3, wherein said drains are connected to separate load devices.

Claim 5. The ohmic resistor as described in claim 3, wherein the channels of said MOSFETs are isolated from each other with channel stoppers.

Claim 6. The ohmic resistor as described in claim 1, wherein the drain of said MOSFET (e.g. pMOS) is connected to the base of a complementary type bipolar junction transistor (e.g. npn BJT), operating as a common emitter amplifier.

Claim 7. The ohmic resistor as described in claim 1, wherein said MOSFET is an nMOS having a drain connected to a pnp BJT current mirror and the output of the current mirror driving the base of an npn common emitter amplifier.

Claim 8. The ohmic resistor as described in claim as described in claim 1, wherein said ohmic resistor is connected to the first base of a BJT differential pair fed from a current source, and a reference voltage connected to the second base of said differential pair.

Claim 9. The ohmic resistor as described in claim 6 further comprising additional BJT differential pairs having said ohmic resistor connected to each base of said additional differential pairs.

Claim 10. The ohmic resistor as described in claim 5, wherein the width ratio of the separate drains is varied to vary inversely the resistance ratio of the resistance mirror.

Claim11. The ohmic resistor as described in claim 1, wherein said gate is applied with a regulating gate voltage derived from said drain-to-source voltage and said drain current so as to satisfy the drain voltage vs current characteristic of a MOSFET.

Claim12. The ohmic resistor as described in claim 11, wherein said regulating gate voltage is derived from a feedback loop.

Claim13. The ohmic resistor as described in claim 12, wherein the source current from a MOSFET applied with a specified dc drain-to source voltage is compared with a reference source current and a compared error output voltage is fed back to the gate of the MOSFET to constitute said adaptive gate voltage for regulating the source current from said MOSFET and the reference source current to be equal.